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REMARKS

The Office Action of 02/20/2007 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

Claims 1-8 were rejected as being anticipated by Sakakibara. Claims 1, 2, 4, 5, 7 and 8 were rejected as being anticipated by Duboc. These rejections are respectfully traversed.

Grounds of distinction of the present invention over Sakakibara and Duboc were communicated perhaps less clearly in the prior response than should have been the case. Applicant apologizes for any confusion that may have been caused thereby.

A feature of the present invention is that a *single base address* is used to define a set of addresses, that set of addresses being used to transmit a data vector to/from a multi-port memory at one time using the set of memory addresses. The feature of using a single base address to define a set of addresses used in this manner may be clearly seen in Fig. 2 of the specification. The base address is supplied on the input AddrIn to multiple different address calculation units (AU) of an Address Configuration Unit (ACU). Each address calculation unit is provided with a register file (RF). The base memory address *supplied in common* to all of the address calculation units is modified by each of the address calculation units individually using information from each address calculation uints register file to obtain a set of addresses (Addr) that is applied to the multi-port memory (MEM).

In Sakakibura, on the other hand, clearly shows in Figs. 1 and 5 that separate base addresses are used for each memory module. Note the base address register 191-1 of Fig. 5, which is replicated four times in Fig. 1 (RQ0, RQ1, RQ2 and RQ3).

In Duboc, there is no base address per se. Rather, each of a plurality of Data Address Generators (Fig. 2, DAG) is provided with a set of indirect address registers (Fig. 4). The indirect address registers are programmed independently for each DAG. For each DAG, one of the indirect address registers is selected in order to access memory.

Accordingly, it may be seen that Skakibara and Duboc both fail to anticipate the present invention.

Withdrawal of the rejections and allowance of claims 1-8 is respectfully requested.

Respectfully submitted,

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